Docket: GS 145 D1

ABSTRACT

A trench DMOS transistor device that comprises: (a) a substrate of a first conductivity type; (b) an epitaxial layer of first conductivity type over the substrate, wherein the epitaxial layer has a lower majority carrier concentration than the substrate; (c) a trench extending into the epitaxial layer from an upper surface of the epitaxial layer; (d) an insulating layer lining at least a portion of the trench; (e) a conductive region within the trench adjacent the insulating layer; (f) a body region of a second conductivity type provided within an upper portion of the epitaxial layer and adjacent the trench; (g) a source region of first conductivity type within an upper portion of the body region and adjacent the trench; and (h) one or more low resistivity deep regions extending into the device from an upper surface of the epitaxial layer. The low resistivity deep region acts to provide electrical contact with the substrate, which is a common drain region for the device. By constructing a trench DMOS transistor device in this fashion, source, drain and gate contacts can all be provided on a single surface of the device.